REMARKS

The Examiner's Action mailed on December 28, 2004 has been received and its contents carefully considered. Claims 1, 4, 5, 8 and 11 have been amended. A new claim 17 has been added. Claims 1-17 are now pending in the application. For at least the following reasons, it is submitted that this application is in condition for allowance.

Claim 5 is rejected under 35 U.S.C. 112, first paragraph. Claim 5 has amended so as clearly to be supported by the specification. The rejection therefore is inapplicable to the amended claim and accordingly should be withdrawn.

Claims 1-16 are rejected under 35 U.S.C. 103 (a) as being unpatentable over the *applicant's admitted prior art (AAPA)* in view of *Takeda* (US Patent 6,326,803). Claim 1 has been amended for improved clarity, and it is submitted that amended claim 1 clearly is patentable over *AAPA* and *Takeda*, whether taken alone or in combination, for at least the following reasons.

Applicant's amended independent claim 1 recites:

> Claim 1 (currently amended): An apparatus of ring-back constriction, coupled to a transmission line, for constricting a ring-back effect, the apparatus comprising:
>
> a comparator, coupled to the transmission line, for comparing a line signal of the transmission line with a reference voltage, and accordingly outputting a comparison signal;
>
> a termination controller, coupled to the comparator, for outputting a termination control signal according to the comparison signal;
>
> a termination variable resistor, coupled to a termination voltage and the transmission line, the resistance of the termination variable resistor being adjusted according to the termination control signal for providing a voltage to the transmission line;

a constriction controller, coupled to the comparator, for outputting a constriction signal; and

a transistor, having a gate and a source, the gate receiving the constriction signal, the transistor being coupled to a constriction voltage and the transmission line, the resistance of the transistor being adjusted according to the voltage difference between the gate and the source;

wherein when the level of the line signal changes from a first voltage level to a second voltage level, the level of the constriction signal successively changes from a third voltage level to a fourth voltage level, maintains the fourth voltage level for a period, and returns to the third voltage level.

Takeda recites:

"In a high level steady state, as was mentioned above, the first primary switch 31 and the first secondary switch 32 are in the OFF state and the ON state, respectively, the second secondary switch 33 and the second primary switch 34 are in the OFF state and the ON the state, respectively, the p-channel MOS transistor 12 and the n-channel MOS transistor 13 are in the ON state and the OFF state, respectively, and the transmission line termination 5 is in the configuration of being connected to the power supply voltage (Vcc) through the medium of the p-channel MOS transistor 12.

If the output of the driver 2 switches to a low level from this state, the voltage level of the transmission line termination 5 switches to a low level, and the first and second primary switches 31, 34 are switched to the ON state and the OFF state, respectively.

At the point in time at which the state of the first and second primary switches 31, 34 are switched, since the output of the delay circuit 20 is held at a low level, the first and second secondary switches 32,33 are held in the ON state and the OFF state, respectively. Therefore, the first primary switch 31 and the first secondary switch 32 both are in the **ON** state, and the second primary switch 34 and the second secondary switch 33 both are in the **OFF** state.

Thus, due to the fact that the first primary switch 31 and the first secondary switch 32 are both in the ON state, the transmission line termination 5 is connected to the power supply voltage Vcc through the medium of the series connected circuit of the first secondary switch 32 and the first primary switch 31, and the potential of the transmission line termination 5 is pulled up to the power supply voltage Vcc side.

Therefore, since the impedance of the terminating circuit 11 is decreased to less than the impedance in a high level stabilized state, the undershoot that is generated when switching from a high level to a low level can be reduced." (emphasis added; see *Takeda*'s col. 9, line 36 to col. 10, line 4, and Fig. 1)

The Examiner views *Takeda*'s inverters (21, 22, and 23), PMOS transistor (32), and NMOS transistor (33) as the constriction controller defined in applicant's claim 1, and views *Takeda*'s PMOS (31) and NMOS transistor (34) as the constriction variable resistor defined in applicant's original claim 1. However, *Takeda*'s inverters (21, 22, and 23) only can output a voltage level **inverse to** the transmission line termination 5, and the signal outputted by the inverters (21, 22, and 23) is used to control PMOS transistor (32) and NMOS transistor (33). Besides, the gates of *Takeda*'s PMOS (31) and NMOS transistor (34) receive the voltage level of the transmission line termination 5.

If only transistor 31 is in the ON state, the transmission line termination 5 is connected to the power supply voltage (Vcc) only through the medium of the p-channel MOS transistor 12. Only when the transistor 31 and 32 both are in the ON state, the transmission line termination 5 is connected to the power supply voltage (Vcc) further

through the medium of transistors 31 and 32, and therefore the impedance of the terminating circuit 11 is reduced.

However, *Takeda* discloses neither that, "the gate (of the transistor) receiving the constriction signal", nor that "when level of the line signal changes from a first voltage level to a second voltage level, the level of the constriction signal successively changes from a third voltage level to a fourth voltage level, maintains the fourth voltage level for a period, and returns to the third voltage level", as recited in the amended claim 1.

Therefore, it would not have been obvious to one of ordinary skill in the art at the time to modify *AAPA* by implementing the technique disclosed by *Takeda* to make the invention defined by the amended claim 1. Amended claim 1 therefore clearly is patentable over *AAPA* in view of *Takeda*.

Claims 2-16 depend from claim 1, and therefore are patentable for at least the reasons advanced above as to the patentability of claim 1.

Based on the above, it is submitted that the application is in condition for allowance, and such a Notice, with allowed claims 1-17, earnestly is solicited.

If the Examiner believes that a further conference would be of value in expediting the prosecution of this application, the Examiner is hereby invited to telephone the

undersigned counsel to arrange for such a conference.

Respectfully submitted,

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Date

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